Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Odd) Examination Dec-2019

CS3CO29 / EC3CO07 / EI3CO07 / IT3CO09 /
OE00005 Digital Electronics /
IT3ES10 Digital Circuit & System

Programme: B.Tech. Branch/Specialisation: All

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. What is decimal equivalent of $(1221)_3$? **1**

(a) 50 (b) 53 (c) 52 (d) 51

ii. Simplify the expression to minimum number of literals ABC+A'B + ABC' **1**

(a) B (b) 1 (c) A' (d) A

iii. The code used for labelling the cells of a K map is **1**

(a) 84-2-1 (b) Hexadecimal

(c) Gray code (d) Octal

iv. The minimum number of 2- input NAND gates required to realize a half adder is **1**

(a) 8 (b) 5 (c) 6 (d) 4

v. A flip flop has two outputs which are **1**

(a) Always 0 (b) Always 1

(c) Always Complementary (d) Always same

vi. While converting a JK flip-flop to D flip-flop instead of connecting an inverter between its J and K inputs a buffer has been connected. The resulting circuit will act as: **1**

(a) JK flip-flop only (b) T flip-flop

(c) D flip-flop (d) None of these

vii. PLA are used to implement **1**

(a) Combinational circuits (b) Sequential circuits

(c) Both (a) and (b) (d) None of these

P.T.O.

viii. A RAM is **1**
(a) Non-volatile memory (b) Volatile memory
(c) Sequential access memory (d) None of these

ix. Which of the following logic families most power efficient? **1**
(a) TTL (b) CMOS (c) RTL (d) DTL

x. TTL is a family of logic circuits built from **1**
(a) JFETs (b) BJTs (c) Resistors (d) BJTs and resistors

Q.2 i. Find the value of base r if $(121)r = (144)_8$. **2**

ii. Why binary number representation is appropriate to handle electronic circuits? **3**

iii. Design a 3-bit binary to excess-3 code converter using K-map method. **5**

OR iv. Find out simplified logic expression for $f(A,B,C,D) = \Sigma m(0,5,6,7,9,10,13,14,15)$ using Quine McClusky minimization procedure. **5**

Q.3 i. Draw block level description with appropriate peripheral gates, of a four bit Adder-Subtractor. Describe operation in brief. **4**

ii. Design a three bit magnitude comparator using required number of blocks of one bit magnitude comparators, each having two input lines and three output bearing usual meanings. Explain connections in brief. **6**

OR iii. Design and implement logic function for carry output of full adder using appropriate multiplexer. **6**

Q.4 i. Draw logic diagram of JK flip-flop with NOR based basic unit, explain working and derive characteristic equation from truth table. Also write excitation table of the same. **4**

ii. Explain Ring Counter with block diagram and state diagram. **6**

OR iii. Explain Johnson Counter with block diagram and state diagram. **6**

Q.5 i. What is ROM? Describe its application to design combinational circuit using any logic function example. **4**

ii. Describe the method of design of logic function with Programmable Logic Arrays. **6**

OR iii. Compare and contrast RAM and ROM based on any three features. **6**

Q.6 Attempt any two:

i. Explain TTL logic family with circuit diagram of basic unit and working. **5**

ii. Explain CMOS logic family with circuit diagram of basic unit and working. **5**

iii. Explain how logic HIGH and no connection inputs are equivalent in TTL family ICs. **5**

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Marking Scheme
CS3CO29 / EC3CO07 / EI3CO07 / IT3CO09 / OE00005
Digital Electronics /
IT3ES10 Digital Circuit & System

Q.1	i.	What is decimal equivalent of $(1221)_3$? (c) 52	**1**
	ii.	Simplify the expression to minimum number of literals ABC+A'B + ABC' (a) B	**1**
	iii.	The code used for labelling the cells of a K map is (c) Gray code	**1**
	iv.	The minimum number of 2- input NAND gates required to realize a half adder is (b) 5	**1**
	v.	A flip flop has two outputs which are (c) Always Complementary	**1**
	vi.	While converting a JK flip-flop to D flip-flop instead of connecting an inverter between its J and K inputs a buffer has been connected. The resulting circuit will act as: (b) T flip-flop	**1**
	vii.	PLA are used to implement (a) Combinational circuits	**1**
	viii.	A RAM is (b) Volatile memory	**1**
	ix.	Which of the following logic families most power efficient? (b) CMOS	**1**
	x.	TTL is a family of logic circuits built from (d) BJTs and resistors	**1**
Q.2	i.	Find the value of base r if $(121)r = (144)_8$.	**2**
		Correct method — 1 mark	
		Correct answer — 1 mark	
	ii.	Why binary number representation is appropriate to handle electronic circuits?	**3**
	iii.	Design a 3-bit binary to excess-3 code converter using K-map method	**5**
		Correct expressions — 4 marks	
		Logic diagram — 1 mark	
OR	iv.	Find out simplified logic expression	**5**
		Correct procedure — 3 marks	
		Correct answer — 2 marks	
Q.3	i.	Four bit Adder-Subtractor	**4**
		Description — 2 marks	
		Diagram — 2 marks	
	ii.	Design a three bit magnitude comparator	**6**
		Description — 2 marks	
		Diagram — 4 marks	
OR	iii.	Design and implement logic function for carry output of full adder using appropriate multiplexer	**6**
		Truth table — 1 mark	
		Multiplexer selection — 1 mark	
		Mux design table — 2 marks	
		Block diagram and connections — 2 marks	
Q.4	i.	JK flip-flop with NOR based basic unit	**4**
		Logic diagram — 1 mark	
		Truth table and K map — 1 mark	
		Characteristic equation — 1 mark	
		Excitation table — 1 mark	
	ii.	Ring Counter	**6**
		Block diagram — 2 marks	
		State diagram — 2 marks	
		Proper explanation — 2 marks	
OR	iii.	Johnson Counter	**6**
		Block diagram — 2 marks	
		State diagram — 2 marks	
		Proper explanation — 2 marks	
Q.5	i.	Definition of ROM — 2 marks	**4**
		Example — 2 marks	
	ii.	Method explanation — 4 marks	**6**
		Diagrammatic explanation — 2 marks	
OR	iii.	RAM and ROM based on any three features	**6**
		2 marks for each features — (2 marks * 3)	

Q.6		Attempt any two:		
	i.	TTL logic family		**5**
		Circuit diagram of basic unit	2 marks	
		Working	3 marks	
	ii.	CMOS logic family		**5**
		Circuit diagram of basic unit	2 marks	
		Working	3 marks	
	iii.	Logic HIGH and no connection inputs are equivalent in TTL family ICs.		**5**
		Circuit diagram	2 marks	
		Explanation	3 marks	

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